

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

5 a first receiver including a first clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated;

10 a first transmitter including a first serializer which converts parallel data into serial data synchronized with one of a transmit clock and the clock generated by the first clock data recovery circuit;

15 a second receiver including a second clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated; and

a second transmitter including a second serializer which converts parallel data into serial data synchronized with one of a transmit clock and the clock generated by the second clock data recovery circuit.

20 2. The device according to claim 1, wherein the first and second transmitters are arranged between the first and second receivers, and

the first and second transmitters are adjacent to the first and second receivers, respectively.

25 3. The device according to claim 1, wherein the first and second receivers are arranged between the first and second transmitters, and

the first and second receivers are adjacent to the first and second transmitters, respectively.

4. The device according to claim 2, further comprising:

5 a first loop-back path which loops serial data from the first transmitter back to the second receiver; and

 a second loop-back path which loops serial data from the second transmitter back to the first receiver,

10 wherein the first and second loop-back paths are formed in a semiconductor integrated circuit device chip.

5. The device according to claim 3, further comprising:

15 a first loop-back path which loops serial data from the first transmitter back to the second receiver; and

 a second loop-back path which loops serial data from the second transmitter back to the first receiver,

20 wherein the first and second loop-back paths are formed in a semiconductor integrated circuit device chip.

6. The device according to claim 1, wherein the first and second transmitters are arranged between the first and second receivers, and

25 the first and second transmitters are adjacent to the second and first receivers, respectively.

7. The device according to claim 1, wherein
the first and second receivers are arranged
between the first and second transmitters, and

the first and second receivers are adjacent to the
5 second and first transmitters, respectively.

8. The device according to claim 4, further
comprising:

a third loop-back path which loops serial data
from the first transmitter back to the first receiver;
10 and

a fourth loop-back path which loops serial data
from the second transmitter back to the second
receiver,

wherein the third and fourth loop-back paths are
15 formed in the semiconductor integrated circuit device
chip.

9. The device according to claim 5, further
comprising:

a third loop-back path which loops serial data
20 from the first transmitter back to the first receiver;
and

a fourth loop-back path which loops serial data
from the second transmitter back to the second
receiver,

25 wherein the third and fourth loop-back paths are
formed in the semiconductor integrated circuit device
chip.

10. The device according to claim 6, further comprising:

a third loop-back path which loops serial data from the first transmitter back to the first receiver;

5 and

a fourth loop-back path which loops serial data from the second transmitter back to the second receiver,

wherein the third and fourth loop-back paths are formed in the semiconductor integrated circuit device chip.

11. The device according to claim 7, further comprising:

a third loop-back path which loops serial data from the first transmitter back to the first receiver;

15 and
a fourth loop-back path which loops serial data from the second transmitter back to the second receiver,

20 wherein the third and fourth loop-back paths are formed in the semiconductor integrated circuit device chip.

12. A semiconductor integrated circuit device comprising:

25 a first receiver including a first clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and

changing a phase of a clock to be generated on the basis of a frequency offset between the received serial data and a reference clock, or first phase control information for controlling a phase of a clock, and
5 a first deserializer which converts serial data synchronized with the generated clock into parallel data;

a first transmitter including a first serializer which converts parallel data into serial data
10 synchronized with one of a transmit clock and the clock generated by the first clock data recovery circuit;

a second receiver including a second clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and
15 changing a phase of a clock to be generated on the basis of a frequency offset between the received serial data and a reference clock, or second phase control information for controlling a phase of a clock, and
a second deserializer which converts serial data
20 synchronized with the generated clock into parallel data; and

a second transmitter including a second serializer which converts parallel data into serial data synchronized with one of a transmit clock and the clock
25 generated by the second clock data recovery circuit.

13. The device according to claim 12, wherein
when the second receiver is to be tested,

the first clock data recovery circuit changes a phase of a clock to be generated on the basis of the first phase control information, and outputs the phase-changed clock to the first transmitter,

5 the first transmitter transmits, to the second clock data recovery circuit, serial data synchronized with the phase-changed clock output from the first clock data recovery circuit, and

10 the second clock data recovery circuit receives the serial data transmitted from the first transmitter, and recovers the clock from the received serial data, and

when the first receiver is to be tested,

15 the second clock data recovery circuit changes a phase of a clock to be generated on the basis of the second phase control information, and outputs the phase-changed clock to the second transmitter,

20 the second transmitter transmits, to the first clock data recovery circuit, serial data synchronized with the phase-changed clock output from the second clock data recovery circuit, and

the first clock data recovery circuit receives the serial data transmitted from the second transmitter, and recovers the clock from the received serial data.

25 14. The device according to claim 12, further comprising:

a test control pattern generator; and

a test analyzer,

wherein the test control pattern generator
generates the first and second phase control
information, and

5 the test analyzer analyzes a state of the second
clock data recovery circuit on the basis of the first
phase control information and phase information of
the clock recovered by the second clock data recovery
circuit, and analyzes a state of the first clock data
10 recovery circuit on the basis of the second phase
control information and phase information of the clock
recovered by the first clock data recovery circuit.

15. The device according to claim 14, wherein

 the test control pattern generator comprises a
15 first test control pattern generating circuit which
generates the first phase control information, and a
second test control pattern generating circuit which
generates the second phase control information, and

 the test analyzer comprises a first test analyzing
20 circuit which analyzes the state of the first clock
data recovery circuit, and a second test analyzing
circuit which analyzes the state of the second clock
data recovery circuit.

16. The device according to claim 12, wherein

25 the first and second transmitters are arranged
between the first and second receivers, and

 the first and second transmitters are adjacent to

the first and second receivers, respectively.

17. The device according to claim 12, wherein
the first and second receivers are arranged
between the first and second transmitters, and

5 the first and second receivers are adjacent to the
first and second transmitters, respectively.

18. The device according to claim 12, wherein
the first and second transmitters are arranged
between the first and second receivers, and

10 the first and second transmitters are adjacent to
the second and first receivers, respectively.

19. The device according to claim 12, wherein
the first and second receivers are arranged
between the first and second transmitters, and

15 the first and second receivers are adjacent to the
second and first transmitters, respectively.

20. A test method for a semiconductor integrated
circuit device comprising

20 a first receiver including a first clock data
recovery circuit capable of receiving serial data,
recovering a clock from the received serial data, and
changing a phase of a clock to be generated,

a first transmitter including a first serializer
which converts parallel data into serial data
25 synchronized with one of a transmit clock and the clock
generated by the first clock data recovery circuit,

a second receiver including a second clock data

recovery circuit capable of receiving serial data,
recovering a clock from the received serial data, and
changing a phase of a clock to be generated, and

5 a second transmitter including a second serializer
which converts parallel data into serial data
synchronized with one of a transmit clock and the clock
generated by the second clock data recovery circuit,
comprising:

when testing the first receiver,
10 causing the second clock data recovery circuit to
change a phase of a clock to be generated regardless of
serial data, and output the phase-changed clock to the
second transmitter;

transmitting serial data synchronized with the
15 phase-changed clock from the second transmitter to the
first clock data recovery circuit;

causing the first clock data recovery circuit to
receive the serial data transmitted from the second
transmitter, and recover the clock from the received
20 serial data; and

analyzing a state of the first clock data recovery
circuit on the basis of phase control information of
the clock changed by the second clock data recovery
circuit, and phase control information when the first
25 clock data recovery circuit recovers the clock, and

when testing the second receiver,
causing the first clock data recovery circuit to

change a phase of a clock to be generated regardless of serial data, and output the phase-changed clock to the first transmitter;

transmitting serial data synchronized with the
5 phase-changed clock from the first transmitter to the second clock data recovery circuit;

causing the second clock data recovery circuit to receive the serial data transmitted from the first transmitter, and recover the clock from the received
10 serial data; and

analyzing a state of the second clock data recovery circuit on the basis of phase control information of the clock changed by the first clock data recovery circuit, and phase control information
15 when the second clock data recovery circuit recovers the clock.